Spacecat iCEDIP v0

All GND pins are connected together internally.

VCCIO0 and VCCIO2 set the IO voltage levels of pin banks 0 and 2 of the FPGA. VCCIO1 is connected to +3.3V.

The recommended VCCIO0,2 voltage range is 1.71V to 3.46V.

Do not exceed these IO currents (per-pin):
@ LVCMOS 3.3V: 8mA sink/source
@ LVCMOS 2.5V: 6mA sink/source
@ LVCMOS 1.8V: 4mA sink/source

	GND	1	1	40	40	GND	
	VCCIO0_EXT	2	2	39	39	+3V3	
	VCCIO2_EXT	3	3	38	38	PGOOD	
27	IOB0_38B	4	4	37	37	IOB0_39A	26
28	IOB0_41A	5	5	36	36	IOB0_36B	25
31	IOB0_42B	6	6	35	35	IOB0_37A	23
32	IOB0_43A	7	7	34	34	IOB1_23B	21
34	IOB0_44B	8	8	33	33	IOB1_25BG	20
35	IOB0_46BG	9	9	32	32	IOB1_29B	19
37	IOB0_45AG	10	10	31	31	IOB1_31B	18
36	IOB0_48B	11	11	30	30	IOB1_24A	13
	GND	12	12	29	29	GND	
38	IOB0_50B	13	13	28	28	IOB1_22A	12
42	IOB0_51A	14	14	27	27	IOB1_20A	11
43	IOB0_49A	15	15	26	26	IOB1_18A	10
44	IOB2_3BG	16	16	25	25	IOB1_16A	9
45	IOB2_5B	17	17	24	24	IOB1_13B	6
46	IOB2_0A	18	18	23	23	IOB2_8A	4
47	IOB2_2A	19	19	22	22	IOB2_9B	3
48	IOB2_4A	20	20	21	21	IOB2_6A	2

Main power input.
2.9V to 3.45V, 3.3V typical.

PGOOD is switched to +3V3 after FPGA power has been sequenced. On some early boards (with 3 chips in-line at the back instead of 4), the PGOOD line may be shorted to +3V3 permanently with a wire link.

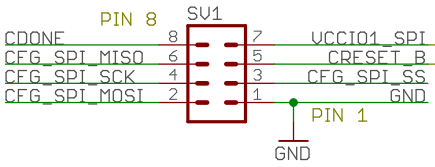
Yellow numbers = pin numbers of the SG48 package.
You'll need to use these in the Pin Constraints Editor of the Lattice iCEcube2 software.

IOBx_yAG = Pad y belonging to IO bank x.

A and B of adjacent numbers can be used as diff pairs. See iCE5LP4K pinout documentation.
G suffix = routable to global clock networks.

For more info, see Lattice iCE5LP1K documentation.

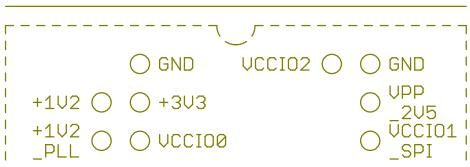
Flash Programming Header

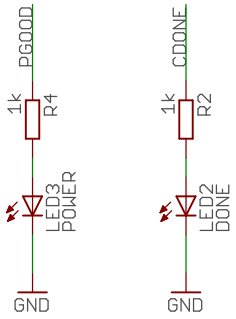


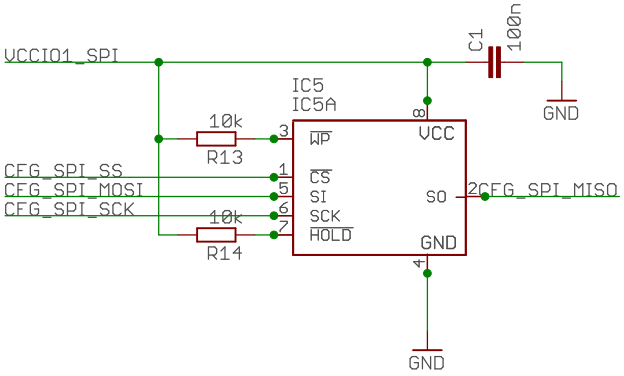
Warning:
VCCIO1_SPI is not there to power the device, but to be used as a reference. SPI flash should ideally be programmed while the board is powered via the +3V3 lines and CRESET_B is held low.

Pull LOW to hold FPGA in reset.

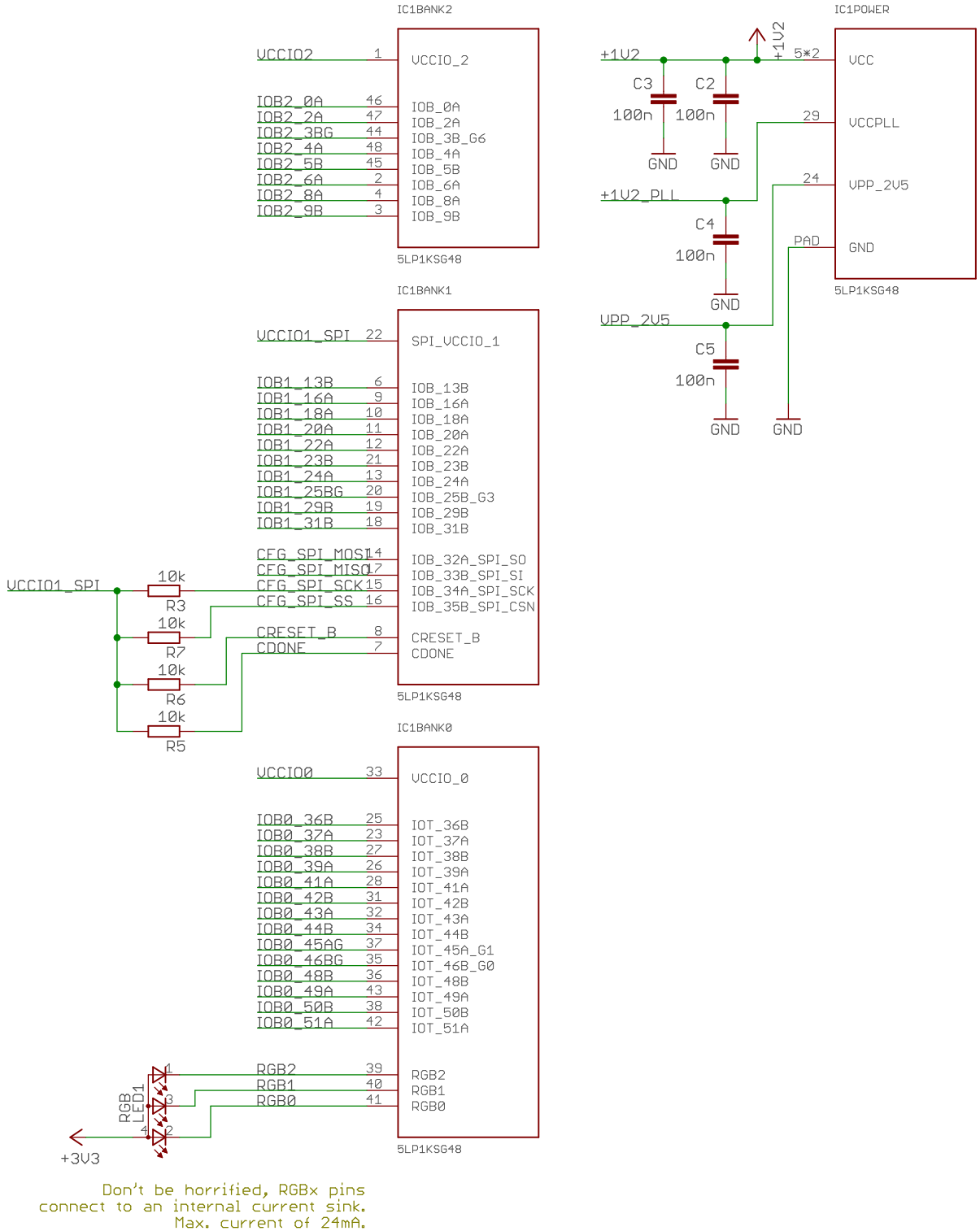
Test Points







Date: 11/06/2022 00:50	
TITLE: main-v0	Sheet: 1/3



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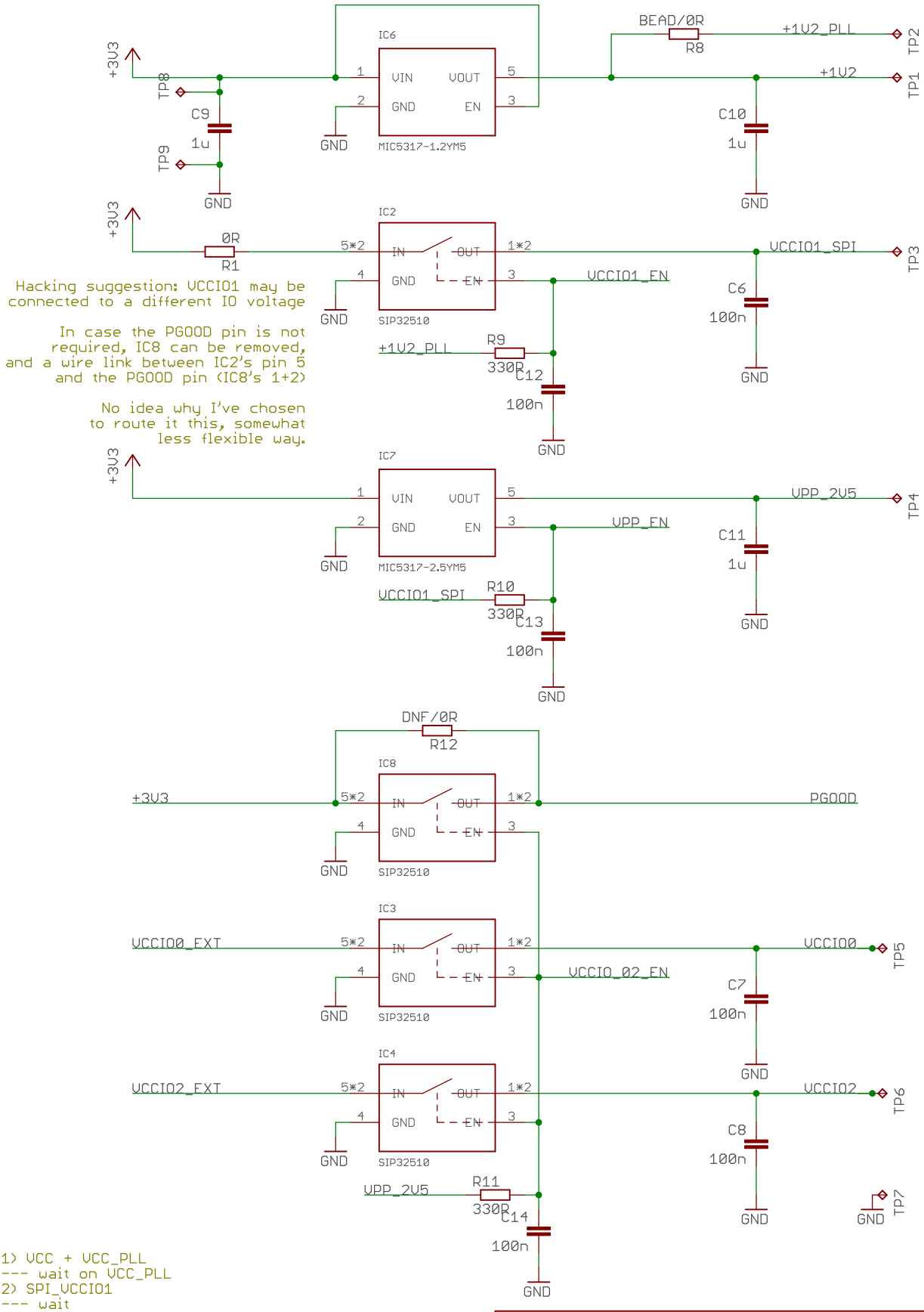
TITLE: main-v0	Sheet: 2/3


+3V3
TP8
C9
1u
TP9
GND
IC6
VIN
VOUT
GND
EN
MIC5317-1.2YM5
BEAD/0R
R8
+1V2_PLL
TP2
+1V2
TP1
C10
1u
GND
+3V3
0R
R1
IC2
IN
OUT
GND
EN
SIP32510
VCCIO1_SPI
TP3
VCCIO1_EN
C6
100n
+1V2_PLL
R9
330R
C12
100n
GND
Hacking suggestion: VCCIO1 may be connected to a different IO voltage
In case the PGOOD pin is not required, IC8 can be removed, and a wire link between IC2's pin 5 and the PGOOD pin (IC8's 1+2)
No idea why I've chosen to route it this, somewhat less flexible way.
+3V3
IC7
VIN
VOUT
GND
EN
MIC5317-2.5YM5
VPP_2V5
TP4
VPP_EN
C11
1u
VCCIO1_SPI
R10
330R
C13
100n
GND
DNF/0R
R12
IC8
IN
OUT
GND
EN
SIP32510
+3V3
PGOOD
IC3
VCCIO0_EXT
VCCIO0
TP5
VCCIO_02_EN
C7
100n
IC4
VCCIO2_EXT
VCCIO2
TP6
C8
100n
VPP_2V5
R11
330R
C14
100n
TP7
1) VCC + VCC_PLL
--- wait on VCC_PLL
2) SPI_VCCIO1
--- wait
3) VPP
--- wait
4) VCCIO0 + VCCIO2
Date: 11/06/2022 00:50
TITLE: main-v0
Sheet: 3/3